



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of)

Patel et al.)

Serial No. 10/750,342)

Filed: December 31, 2003)

For: IDENTIFYING PROCESS AND
TEMPERATURE OF SILICON
CHIPS

) Group No. 2857

SECOND REQUEST FOR CORRECTION OF OFFICIAL FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: OFFICE OF INITIAL PATENT EXAMINATION'S CUSTOMER SERVICE CENTER

Dear Sir:

Applicant hereby submits a copy of the Request for Correction of Official Filing Receipt previously filed August 27, 2004, with attachments. Applicant received a response to our initial Request for Corrected Filling Receipt requesting that Applicant submit an amendment to the first page of the specification adding the claim to priority. No amendment to the first page of the specification should be necessary, as Applicant correctly claimed priority when the application was initially filed (please see attached copy of the first page of specification as originally filed.)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:

October 15, 2004

(Date of Deposit)

Theresa Badet

(Name of the Person Making Deposit)

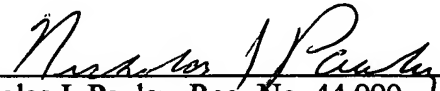
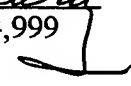
Theresa Badet
(Signature)

Applicants submit that the above-indicated error is an error made on the part of the Office, rather than by the Applicants, and respectfully request that the noted error in the priority claim of the application be corrected and a new Official Filing Receipt be issued to Applicants.

Respectfully submitted,

Dated: October 15, 2004

By:


Nicholas J. Pauley, Reg. No. 44,999
Phone No. (858) 845-8405 

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-5787
Facsimile: (858) 658-2502

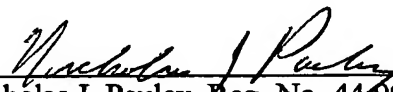
Enclosed herewith is a copy of the Combined Declaration/Power of Attorney filed on June 30, 2004. As listed on the Combined Declaration/Power of Attorney, the application claims priority to 60/525,103 filed November 24, 2003 AND 10/722,350 filed November 25, 2003.

Also enclosed, is a copy of the first page of patent application indicating the priority claim as well as a copy of the incorrect Official Filing Receipt showing the correction to me made in red ink.

Applicants submit that the above-indicated error is an error made on the part of the Office, rather than by the Applicants, and respectfully request that the noted error in the priority claim of the application be corrected and a new Official Filing Receipt be issued to Applicants.

Respectfully submitted,

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COPY

IDENTIFYING PROCESS AND TEMPERATURE OF SILICON CHIPS

BACKGROUND

[0000] This application claims priority to U.S. Provisional Application Serial No. 60/525,103, filed November 24, 2003 and U.S. Application Serial No. 10/722,350, filed November 25, 2003.

Field

[0001] The present disclosure relates to systems and techniques for identifying process and temperature of chips.

Background

[0002] The demand for wireless services has led to the development of an ever increasing number of chips, all of which must adhere to strict industry performance standards. Manufacturing of silicon chips is guided in part by standards and tolerances for nominal process speed. Within the guidelines of such standards, chips are designed to run at their rated clock speed for their entire expected lifetime, even in worst-case temperature and voltage conditions. Thus, part of the manufacturing process includes testing manufactured chips to identify their rated clock speed and ensure they are rated properly.

[0003] Chips for use in communications devices must generally be rated to operate at a specified nominal speed, within a certain allowed tolerance. However, a set of chips generated from a single wafer commonly will fall into a range of different process speed ratings.

[0004] In an attempt to use those portions of the wafer that produce different speed ratings, some manufacturers engage in a method of speed binning, in which the various chips produced from a single wafer are tested and batched according to their graded process speed. Batching chips according to their speed may be time consuming and costly.

[0005] Some manufacturers may even discard slow chips and fast chips that are outside of the nominal tolerance range. For example, SDRAM chips require an external clock from the host controller with control and data signals. Because the host clock is sensitive to



COMBINED DECLARATION / POWER OF ATTORNEY

AS BELOW NAMED INVENTOR, I HEREBY DECLARE THAT: This Declaration is of the following type:

- ☒ Original ☐ Supplemental ☐ Continuation-In-Part ☐ Divisional
☐ Continuation ☐ National Stage of PCT

My residence, post office address and citizenship are as stated below next to my name: I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention IDENTIFYING PROCESS AND TEMPERATURE OF SILICON CHIPS, the specification of which:

- ☐ is attached hereto.
☒ was filed on December 31, 2003 as Serial No. 10/750,342.
☐ was amended on _____ (if applicable).
☐ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 of any foreign application(s) for patent or inventor's certificate or of any PCT International application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

Priority Claimed

(Country)	(Application No.)	(Day/Month/Year/Filed)	(Yes)	(No)
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I hereby claim the benefit under Title 35 USC 119(e) of any United States provisional application(s) listed below:

60/525,103	November 24, 2003
(Serial No.)	(Filing Date)
10/722,350	November 25, 2003
(Serial No.)	(Filing Date)

I hereby claim the benefit under Title 35 USC 120 of the United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 USC 112, I acknowledge the duty to disclose material information as defined in Title 37 CFR 1.56(a) which occurred between the filing date of the prior application and the national or PCT International filing date of this application:

(Serial No.)	(Filing Date)	(Status)
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I hereby appoint the attorneys and/or agents associated with Customer No. 23696 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith. Please direct all telephone calls to Philip R. Wadsworth at (858) 651-4404 and address all correspondence to: QUALCOMM Incorporated, Patent Department, 5775 Morehouse Drive, San Diego, California 92121-1714.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Joint Inventor Jagrut Viliskumar Patel	Inventor Signature <i>J.V. Patel</i>	Date 19-6-2004
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Full Name of Second or Joint Inventor Martin Vyungchon Choe	Inventor Signature <i>M. Vyungchon Choe</i>	Date 21-6-2004
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Full Name of Third or Joint Inventor Ziad Mansour	Inventor Signature <i>Ziad Mansour</i>	Date JUNE 28, 2004
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UNITED STATES PATENT AND TRADEMARK OFFICE

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 United States Patent and Trademark Office
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 Alexandria, Virginia 22313-1450
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APPL NO.	FILING OR 371 (c) DATE	PART UNIT TRADEMARK	FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/750,342	12/31/2003	2857	1202	030439	7	32	4

CONFIRMATION NO. 9469

23696

 Qualcomm Incorporated
 Patents Department
 5775 Morehouse Drive
 San Diego, CA 92121-1714

UPDATED FILING RECEIPT



OC000000013412885

Date Mailed: 08/02/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

 Jagrut Viliskumar Patel, San Diego, CA;
 Martin Vyungchon Choe, San Diego, CA;
 Ziad Mansour, Poway, CA;

COPY

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/525,103 11/24/2003

10/720,350 11/25/2003

Foreign Applications

If Required, Foreign Filing License Granted: 05/03/2004

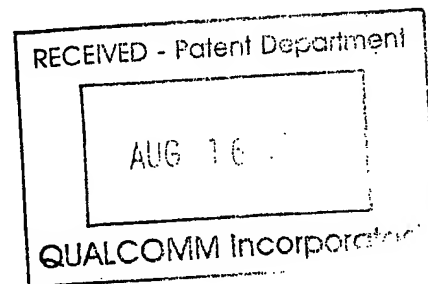
Projected Publication Date: 05/26/2005

Non-Publication Request: No

Early Publication Request: No

Title

Identifying process and temperature of silicon chips



COPY

Preliminary Class

702

**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

GRANTED

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).